IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/652,550
Priority Filing Date ..... August 31, 2000
Inventor ..... Keiji Jono et al.
Assignee ..... Micron Technology, Inc. and KMT Semiconductor, LTD
Priority Group Art Unit 2811
Priority Examiner ..... T. Tran
Attorney's Docket No. KM1-003
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS

INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending Application Serial No. 09/652,550, filed August 31, 2000, upon which the above-identified application relies for a priority date under 35 U.S.C. §120. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). As a courtesy, Applicant submits copies of the cited article references for review.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: Nov. 8, 2001

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